NOORUL ISLAM CENTRE FOR HIGHER EDUCATION

(Deemed to be University Under Section 3 of the UGC Act, 1956)
Kumaracoil, Thuckalay

DEPARTMENT OF

ELECTRICAL ANDELECTRONICS ENGINEERING

M.E. APPLIED ELECTRONICS

CURRICULUM AND SYLLABI

REGULATION 2023

NOORUL ISLAM CENTRE FOR HIGHER EDUCATION
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Regulation : 2023

Curriculum and Syllabi

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

M.E – APPLIED ELECTRONICS

Vision of the University

To be recognized by the Government and society at large as an institution able to deliver excellence with relevance in the field of higher education and research focusing on the needs of the nation in tune with the technological revolution to cope with the knowledge explosion and global competence.

Mission of the University

To develop the institution as a Centre of Excellence, keeping pace with the advances in the field, so as to provide quality higher education to the students and instill in them high standards of discipline and ethics so that they become enlightened individuals in the service of humanity and to carry out focused research in the frontier areas of science and technology.

Faculty of Electrical Engineering

Department of Electrical and Electronics Engineering

Vision of the Department

To evolve into a nationally recognized department in the frontier areas of Electrical and Electronics Engineering and to be recognized by the government and society at large and by the industry and commerce in particular as an institution able to deliver excellence with relevance in the field of technical education focusing on the needs of the nation in tune with the technological revolution.

Mission of the Department

To produce Electrical and Electronics Engineering graduates having professional excellence, to provide technical support to budding entrepreneurs and existing industry and to Develop the institution as a centre of Excellence , keeping pace with advances in the field, so as to provide quality higher Education to the students and instill in them high standards of discipline and ethics so that they become enlightened

individuals in the service of humanity and to carry out focused research in the frontier areas of science and technology.

Programme Educational Objectives - PEO	
PEO-01	The engineers of Applied Electronics, design circuits and develop systems in contemporary and frontier areas of electronics.
PEO-02	The enhanced skills of the engineers meet the demands and expectations of automation in various industries.
PEO-03	The graduates with professional competency promote and support creative research and developmental activities.

Graduate Attributes-GA	
GA-1	**Advanced Engineering Expertise** Master advanced engineering principles and apply them to design, analyze, and innovate systems that address both present and emerging global challenges across diverse industries.
GA-2	**Leadership in Research and Innovation** Lead groundbreaking research and foster innovation by identifying opportunities for technological advancements, contributing original ideas that push the boundaries of engineering knowledge.
GA-3	**Sustainable Engineering Practices** Develop and implement engineering solutions that integrate sustainability, environmental stewardship, and resource efficiency, ensuring the long-term impact and responsibility of all projects.
GA-4	**Ethical and Strategic Decision-Making** Make informed, ethical decisions in complex engineering contexts, considering societal needs, environmental implications, and the long-term consequences of engineering practices.
GA-5	**Global Competence in Engineering Solutions** Exhibit a deep understanding of global engineering standards and practices, addressing international challenges and cultural sensitivities in engineering projects to make a broader societal impact.
GA-6	**Technological Agility and Lifelong Learning** Stay ahead of technological trends and exhibit agility in learning new tools, methodologies, and technologies, ensuring continuous professional growth in a rapidly evolving engineering landscape.
GA-7	**Interdisciplinary and Collaborative Innovation** Excel in multidisciplinary collaborations, leveraging knowledge from multiple fields to solve complex, large-scale engineering problems that require comprehensive and innovative solutions.
GA-8	**Data-Driven Decision Making** Employ advanced data analytics, machine learning, and computational tools to derive insights and make informed engineering decisions that improve performance, efficiency,

GA-9	**Entrepreneurial Mindset and Innovation Leadership** Cultivate an entrepreneurial mindset, translating engineering innovations into viable products, solutions, or services, and leading teams toward commercialization and societal impact.
GA-10	**Safety, Risk, and Crisis Management** Implement and manage advanced safety protocols and risk mitigation strategies to protect individuals, communities, and ecosystems in engineering practices, particularly in high-stakes and crisis environments.

Programme Outcome - PO	
PO-A	An ability to integrate knowledge from the fields of study and arrive solutions for complex engineering tasks.
PO-B	An ability to understand different kinds of problem solving methods through the imparted domain knowledge.
PO-C	To solve a broad research competence problem systematically, to analyze the reasonable value of new ideas and technology decisions with confidence.
P0-D	An ability to empower with an in-depth understanding of research orientation in their chosen domain with a strategy.
PO-E	An ability to design an ICT based system for optimal analysis of systems.
PO-F	An ability to stimulate opportunities to contribute skills thereby providing an option to find applications suiting the revolutionized concepts.
PO-G	To research and implement a project that meets the needs within realistic constraints.
PO-H	To inculcate a desire for continuous learning and creativity, with emerging tools and technology.
PO-I	An ability to understand the responsibility of taking professional decisions based on the impact of socio- economic issues.
PO-J	To develop the self-confidence towards the professional competency with interpersonal skills.

PO-K	To develop a skill in conducting research in their chosen field, and present their results and findings in scientific forums.
PO-L	An ability to deliver inspiring thoughts and show unparalleled commitment.

Mapping of Graduate Attributes and Programme Educational Objectives

GAs / PEOs	GA-01	GA-02	GA-03	GA-04	GA-05	GA-06	GA-07	GA-08	GA-09	GA-10	GA-11	GA-12
PEO-1	H	A	A	A	A	A	A	A	A	A	A	A
PEO-2	A	H	H	A	A	A	A	A	A	A	A	A
PEO-3	A	A	A	H	H	A	A	A	A	A	A	A

H- Highly Associated A- Associated Not – Not Associated

Mapping of Graduate Attributes and Programme Outcomes (PO)

GAs / PEOs	GA-01	GA-02	GA-03	GA-04	GA-05	GA-06	GA-07	GA-08	GA-09	GA-10
PO-B	H	H	A	A	A	A	H	Not	H	Not
PO-C	H	H	H	H	H	A	H	Not	H	Not
P0-D	H	H	A	A	H	H	H	Not	A	Not
PO-E	A	A	A	A	A	H	A	Not	A	Not

PO-F	**Not**	**H**	**A**	**A**	**A**	**A**	**H**	**H**	**Not**	**H**
PO-G	**H**	**H**	**H**	**H**	**A**	**H**	**A**	**H**	**Not**	**H**
PO-H	**A**	**H**	**H**	**H**	**H**	**H**	**A**	**H**	**Not**	**H**
PO-I	**A**	**A**	**A**	**A**	**H**	**H**	**H**	**H**	**A**	**H**
PO-J	**Not**	**Not**	**Not**	**Not**	**Not**	**H**	**H**	**H**	**Not**	**H**
PO-K	**H**	**A**	**H**	**H**	**H**	**H**	**H**	**H**	**H**	**A**
PO-L	**H**	**A**	**A**	**A**	**H**	**H**	**H**	**H**	**H**	**A**

H- Highly Associated A- Associated Not – Not Associated

Mapping of Programme Educational Objective (PEOs) and Programme Outcomes (POs)

PEO / PO	PEO-01	PEO-02	PEO-03
PO-A	H	A	A
PO-B	A	H	A
PO-C	A	A	H
P0-D	A	A	H
PO-E	A	H	A

PO-F	A	H	A
PO-G	A	H	A
PO-H	A	A	H
PO-I	A	H	H
PO-J	A	A	H
PO-K	H	A	H
PO-L	A	H	A

H- Highly Associated A- Associated Not – Not Associated

Duration of the Programme: 2 Years/ 4 Semesters

Total credit: 68

CURRICULUM & SYLLABUS

SEMESTER I

SI. NO	COURSE CODE	COURSE TITLE	L	T	P	C
THEORY						
1.	MA4501	Advanced Mathematics	3	1	0	4
2.	EE4501	Advanced Digital Signal Processing	3	0	0	3
3.	EE4502	Advanced Digital System Design	3	0	0	3
4.	EE4503	Advanced Microprocessor and Microcontroller	3	0	0	3
5.	EExxx	Elective-I	3	0	0	3
6.	EExxx	Elective – II	3	0	0	3
PRACTICAL						
7.	EE4571	Electronic System Design Lab-I	0	0	2	1
Total			**18**	**1**	**2**	**20**

SEMESTER II

SI. NO	COURSE CODE	COURSE TITLE	L	T	P	C
THEORY						
1.	EE4504	Analysis and Design of Analog Integrated Circuits	3	0	0	3
2.	EE4505	Semiconductor Devices and Modelling	3	0	0	3
3.	EE4506	Digital Control Engineering	3	0	0	3

4.	EE4507	Advanced Embedded Systems	3	0	0	3
5.	EExxx	Elective-III	3	0	0	3
6.	EExxx	Elective- IV	3	0	0	3
PRACTICAL						
7.	EE4572	Electronic System Design Laboratory-II	0	0	2	1
Total			**18**	**0**	**2**	**19**

SEMESTER III

SI. NO	**COURSE CODE**	**COURSE TITLE**	**L**	**T**	**P**	**C**
THEORY						
1.	EExxxx	Elective-IV	3	0	0	3
2.	OE-I	Open Elective-I	3	0	0	3
PRACTICAL						
3.	EE45P1	Project Work Phase-I	0	0	18	6
Total			**6**	**0**	**18**	**12**

SEMESTER IV

SI. NO	**COURSE CODE**	**COURSE TITLE**	**L**	**T**	**P**	**C**
PRACTICAL						
7.	EE45P2	Project Work Phase-II	**0**	**0**	**32**	**16**

LIST OF PROGRAM ELECTIVES

SI. NO.	COURSE CODE	COURSE TITLE	L	T	P	C
1.	EE45A1	Robotics	3	0	0	3
2.	EE45A2	Electromagnetic Interference and Compatibility in System Design	3	0	0	3
3.	EE45A3	Low Power VLSI	3	0	0	3
4.	EE45A4	Internet Working and Multimedia	3	0	0	3
5.	EE45A5	DSP Integrated Circuits	3	0	0	3
6.	EE45A6	High Speed Switching Architecture	3	0	0	3
7.	EE45A7	CADD for VLSI Circuits	3	0	0	3
8.	EE45A8	Data Converters	3	0	0	3
9.	EE45A9	Machine Learning	3	0	0	3
10.	EE45B1	Digital Image Processing and Applications	3	0	0	3
11.	EE45B2	VLSI Design	3	0	0	3
12.	EE45B3	High Performance Communication Networks	3	0	0	3
13.	EE45B4	Embedded Analog Interfacing	3	0	0	3

SEMESTER I

SI. NO	COURSE CODE	COURSE TITLE	L	T	P	C
THEORY						
1.	MA4501	Advanced Mathematics	3	1	0	4
2.	EE4501	Advanced Digital Signal Processing	3	0	0	3
3.	EE4502	Advanced Digital System Design	3	0	0	3
4.	EE4503	Advanced Microprocessor and Microcontroller	3	0	0	3
5.	EExxx	Elective-I	3	0	0	3
6.	EExxx	Elective – II	3	0	0	3
PRACTICAL						
7.	EE4571	Electronic System Design Lab-I	0	0	2	1
Total			**18**	**1**	**2**	**20**

MA4501	ADVANCED MATHEMATICS	L	T	P	C
		3	1	0	4

AIM:

To gain a well-found knowledge of optimizing a function and variation problems which provide necessary mathematical support and confidence to tackle real life problems.

OBJECTIVE:

The course objective is, the students will be able to apply various methods in Linear Algebra to solve

the system of linear equations, use two-dimensional random variables, and correlations in solving application problems apply the ideas of Random Processes and understand the basic characteristic features of a queueing system and acquire skills in analyzing queueing models.

Subject Code:MA4501	**Subject Name: ADVANCED MATHEMATICS**	
Course Outcome - COs		**Cognitive Skill**
CO-01	Compute various methods in Linear Algebra to solve the system of linear equations. Using generalized eigen vectors, find the inverse of a singular matrix using the Pseudo inverse method.	R, U, A, E, An
CO-02	Formulate real-life problems and solve them using Linear Programming. Minimize the cost of distributing a product from many sources using TP. Assign a job to some workers so that the jobs are completed at the least cost or time.	R, U, A, E, An
CO-03	The random variable needs the analysis of random phenomena. Apply the concept of the moment, moment generating function. Extended one-dimensional random variables to two-dimensional random variables and analyze. Understand the concept of Correlation	R, U, A, E, An
CO-04	Know the concepts which describe the random wave transforms in a probabilistic sense. Trace the nature of random signals. Analyze the random signals in the frequency domain	R, U, A, E, An
CO-05	To understand the basic characteristic features of a queuing system and acquire skills in analyzing queuing models.	R, U, A, E, An

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO-I	PO-J	PO-k	PO-L
CO-01	S	S	S	M	S	M	S	S	M	S	L	L
CO-02	S	M	S	S	M	S	S	S	S	S	L	L
CO-03	S	M	M	S	S	S	S	S	S	M	S	L
CO-04	M	S	M	M	M	M	S	M	S	L	L	M
CO-05	M	S	S	S	M	S	M	S	S	M	S	L

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT I LINEAR ALGEBRA (9)

Vector spaces – Norms – Inner products – Eigenvalues using QR transformations —Generalized eigenvectors – Jordan Canonical forms – Singular value decomposition and applications – Pseudo inverse

UNIT II LINEAR PROGRAMMING (9)

Formulation – Graphical solution – Simplex method: Big M Method– Transportation problems – Assignment models

UNIT III PROBABILITY AND RANDOM VARIABLES (9)

Probability Concepts – Axioms of probability – Conditional probability – Random variables

– Probability functions – Two-dimensional random variables – Joint distributions – Marginal and conditional distributions – Correlation.

UNIT IV RANDOM PROCESSES (9)

Classification – Stationary random processes – Ergodic process - The autocorrelation – Cross Correlations – Properties - Power spectral density, Cross Power spectral density.

UNIT V QUEUING THEORY (9)

Birth and Death process - Markovian queuing models – Little's formulae - M/M/1,M/M/C finite and infinite capacity (steady state solutions only)

L: 45 + T: 15, TOTAL: 60 PERIODS

REFERENCES:

1. Friedberg A.H, Insel A.J. and Spence L, "Linear Algebra", Prentice Hall of India, New Delhi, 2004.
2. Taha, H.A., "Operations Research – An Introduction", Sixth Edition, Prentice-Hall of India, New Delhi.
3. Gupta, P.K. and Hira, D.S., "Operations Research", S.Chand& Co. New Delhi.
4. Peebles Jr., P.Z., "Probability, Random Variables and Random Signal Principles" ,McGraw-Hill Inc.
5. Gross, D., Shortie, J.F., Thompson, J.M and Harris, C.M., "Fundamentals of Queueing Theory", 4th Edition, Wiley,2014.

EE4501	ADVANCED DIGITAL SIGNAL PROCESSING	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To describe fundamental concepts of DSP and Discrete Transforms
- To design digital filters design
- To estimate power spectrum using non- parametric and parametric methods
- To analyze the Multirate Signal processing by decimation and interpolation.
- To apply the concept of Multirate signal processing for various applications

Subject Code: EE4501	Subject Name: Advanced Digital Signal Processing	
Course Outcome - COs		**Cognitive Skill**
CO-01	Describe the basics of Digital Signal Processing and Discrete Time Transforms.	U,R
CO-02	Design and implement FIR/IIR digital filters using various structures	A
CO-03	Estimate power spectrum using appropriate parametric/non-parametric method.	E
CO-04	Analyze discrete time system at different sampling frequencies using the concept of Multirate signal processing	An
CO-05	Design discrete time system for the given application using Multirate signal processing	R,A

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO-I	PO-J	PO-k	PO-L
CO-01	S	S	S	M	L	M	N	N	L	N	M	L
CO-02	S	M	S	S	M	S	N	N	L	N	S	L
CO-03	S	M	M	S	S	L	N	N	L	N	S	L
CO-04	M	L	M	M	M	M	N	N	L	N	L	M
CO-05	M	L	S	S	M	S	N	N	L	N	L	L

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT I DIGITAL SIGNAL PROCESSING 9

Sampling of analog signals - Selection of sampling frequency - Frequency response – Transfer functions- Filter Structures-Fast Fourier Transform (FFT)Algorithms -Image coding-DCT.

UNITII DIGITAL FILTER DESIGN 9

IIR and FIR Filters: Filter structures, Implementation of Digital Filters- 2nd Order Narrow Band Filter and 1st Order All Pass Filter, Frequency sampling structures of FIR, Lattice structures, Forward and Backward prediction error filters, Reflection coefficients for lattice realization, Implementation of lattice structures for IIR filters, Advantages of lattice structures.

UNIT III ESTIMATIONOFPOWERSPECTRUM 9

Non-Parametric Methods: Estimation of spectra from finite duration observation of signals, Bartlett, Welch & Blackman- Tukey methods, Performance Comparison. Parametric Methods: Autocorrelation & Its Properties, Relation between autocorrelation & model parameters, AR Models -Yule-Walker &Burg Methods, MA & ARM A models for power spectrum estimation.

UNIT IV MULTIRATESIGNALPROCESSING 9

Decimation by a factor D - Interpolation by a factor I - Sampling rate conversion by a rational factor I/D, Multistage Implementation of Sampling Rate Conversion, Filter design and Implementation for sampling rate conversion. Up-sampling using All Pass Filter.

UNIT V APPLICATIONS OF MULTI RATE SIGNAL PROCESSING AND DSP INTEGRATED CIRCUITS 9

Design of Phase Shifters, Interfacing of Digital Systems with Different Sampling Rates, Implementation of Narrow Band Low Pass Filters, Implementation of Digital Filter Banks, Subband Coding of Speech Signals, Quadrature Mirror Filters, Over Sampling A/D and D/A Conversion.

TOTAL:45 PERIODS

REFERENCES:

1. J.G. Proakis & D. G. Manolakis Digital Signal Processing: Principles, Algorithms & Applications-,4thEd.,Pearson Education,2013.
2. Alan V Oppenheim & Ronald W Schaffer Discrete Time signal processing, Pearson Education, 2014.
3. Keshab K. Parhi, 'VLSI Digital Signal Processing Systems Design and Implementation ",John Wiley& Sons,2007.
4. Steven. M.Kay, Modern Spectral Estimation: Theory & Application–PHI,2009.
5. P.P.Vaidyanathan, Multi Rate SystemsandFilterBanks,PearsonEducation,1993.
6. Emmanuel C. Ifeachor, Barrie W. Jervis, "Digital Signal Processing–A practical approach", Second Edition,Harlow,PrenticeHall,2011.

EE4502	ADVANCED DIGITAL SYSTEM DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To design a synchronous sequential circuit.
- To learn about hazards in a synchronous sequential circuit.
- To study the fault testing procedure for digital circuits.
- To understand the architecture of programmable devices.
- To design and implement digital circuits using programming tools.

Subject Code: EE4502	**Subject Name: Advanced Digital System Design**	
Course Outcome - COs		**Cognitive Skill**
CO-01	Analyse and design synchronous sequential circuits.	An
CO-02	Analyse hazards and design asynchronous sequential circuits.	An
CO-03	Knowledge on the testing procedure for combinational circuit and PLA.	U
CO-04	Able to design PLD and ROM.	A
CO-05	Design and use programming tools for implementing digital circuits of industry standards.	R,A

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO-I	PO-J	PO-k	PO-L
CO-01	S	S	S	M	L	M	L	L	N	M	L	L
CO-02	S	M	S	S	M	S	L	L	N	M	L	L
CO-03	S	M	M	S	S	S	L	L	N	M	S	L
CO-04	M	S	L	M	N	M	L	L	N	M	L	M
CO-05	M	S	L	S	N	S	L	L	N	L	S	L

S- Strong, M- Medium, L-Low, N- Not Relevant

UNITI SEQUENTIAL CIRCUIT DESIGN 9

Analysis of Clocked Synchronous Sequential Circuits and Modelling-State Diagram, State Table, State Table Assignment and Reduction-Design of Synchronous Sequential Circuits Design of Iterative Circuits-ASM Chart and Realization using ASM.

UNITII ASYNCHRONOUS SEQUENTIALCIRCUITDESIGN 9

Analysis of Asynchronous Sequential Circuit – Flow Table Reduction-Races-State Assignment-Transition Table and Problems in Transition Table- Design of Asynchronous Sequential Circuit -Static, Dynamic and Essential hazards–Mixed Operating Mode Asynchronous Circuits–Designing Vending Machine Controller.

UNITIII FAULTDIAGNOSISANDTESTABILITYALGORITHMS 9

Fault Table Method-Path Sensitization Method – Boolean Difference Method -D Algorithm — Tolerance Techniques – The Compact Algorithm– Fault in PLA – Test Generation – DFT Schemes–Built in Self-Test.

UNITIV SYNCHRONOUS DESIGNUSINGPROGRAMMABLEDEVICES 9

Programming Logic Device Families–Designing a Synchronous Sequential Circuit using PLA /PAL – Designing ROM with PLA – Realization of Finite State Machine using PLD – FPGA –XilinxFPGA-Xilinx4000.

UNITV SYSTEMDESIGNUSINGVERILOG 9

Hardware Modelling with Verilog HDL – Logic System, Data Types And Operators For Modelling In VerilogHDL - Behavioural Descriptions In Verilog HDL–HDL Based Synthesis–Synthesis Of Finite State Machines– Structural Modelling – Compilation And Simulation Of Verilog Code – Test Bench - Realization Of Combinational And Sequential Circuits Using Verilog – Registers – Counters–Sequential Machine–Serial Adder–Multiplier-Divider–Design Of Simple Microprocessor, Introduction To System Verilog.

TOTAL : 45 PERIODS

REFERENCES:

1. Charles H.Roth jr., “Fundamentals of Logic Design” Thomson Learning,2013.
2. M.D.Ciletti , Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall, 1999
3. M.G.Arnold, Verilog Digital – Computer Design, Prentice Hall (PTR), 1999.
4. Nripendra N Biswas “Logic Design Theory” Prentice Hall of India,2001.
5. Paragk.Lala “Fault Tolerant and Fault Testable Hardware Design” B S Publications,2002
6. Paragk.Lala “Digital System Design Using PLD” B S Publications,2003.
7. Palnitkar , Verilog HDL – A Guide to Digital Design and Synthesis, Pearson , 2003.

EE4503	ADVANCED MICROPROCESSOR AND MICRO CONTROLLERS	L	T	P	C
		3	0	0	3

OBJECTIVES

- To do a detailed study of microprocessor architecture.
- To study the Pentium processor in detail.
- To study the ARM processor in detail.
- To do the detailed study of MOTOROLA 68HC11 micro controller.
- To do the detailed study of PIC micro controller.

Subject Code:EE4503 Subject Name: Advanced Microprocessors and micro controllers		
Course Outcome – Cos		**Cognitive Skill**
CO-01	To understand about the microprocessor architecture and its applications	U,A
CO-02	To analyze about the performance of CISE ARCHETECTURE	An
CO-03	To remember the operations of ARM architecture	R
CO-04	To understand about the working of MOTOROLA micro controllers	U
CO-05	To understand the working and applications of PIC microcontrollers	U,A

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO – I	PO-J	PO- k	PO -L
CO-01	S	L	N	S	N	S	S	N	N	N	S	N
CO-02	S	N	M	S	N	L	S	N	N	N	M	N
CO-03	L	S	M	L	N	S	L	N	L	N	S	N
CO-04	S	L	N	L	N	S	S	N	N	N	L	N
CO-05	L	N	N	L	N	S	S	N	N	N	M	N

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT I **9**

MICROPROCESSOR ARCHITECTURE

Instruction Set – Data formats –Addressing modes – Memory hierarchy –register file – Cache – Virtual memory and paging – Segmentation- pipelining –the instruction pipeline – pipeline hazards – instruction level parallelism – reduced instruction set –Computer principles – RISC versus CISC..

UNIT II **9**

HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM

CPU Architecture- Bus Operations – Pipelining – Brach predication – floating point unit- Operating Modes –Paging – Multitasking – Exception and Interrupts – Instruction set – addressing modes – Programming the Pentium processor.

UNIT III **9**

HIGH PERFORMANCE RISC ARCHITECTURE: ARM

Organization of CPU – Bus architecture –Memory management unit - ARM instruction set- Thumb Instruction set- addressing modes – Programming the ARM processor.

UNIT IV **9**

MOTOROLA 68HC11 MICROCONTROLLERS

Instruction set addressing modes – operating modes- Interrupt system- RTC-Serial Communication Interface – A/D Converter PWM and UART.

UNIT V **9**

PIC MICRO CONTROLLER

CPU Architecture – Instruction set – interrupts- Timers- I^2C Interfacing –UART- A/D Converter –PWM and introduction to C-Compilers.

TOTAL: 45 PERIODS

REFERENCES:

1. Daniel Tabak , ‘’ Advanced Microprocessors” McGraw Hill.Inc., 1995
2. James L. Antonakos, “The Pentium Microprocessor ‘’ Pearson Education, 1997.
3. Steve Furber, ‘’ ARM System –On –Chip architecture “Addison Wesley, 2000.
4. Gene .H.Miller.” Micro Computer Engineering,” Pearson Education, 2003.
5. John .B.Peatman, “Design with PIC Microcontroller, Prentice hall, 1997.
6. James L.Antonakos,” An Introduction to the Intel family of Microprocessors ‘’ Pearson Education 1999.
7. Barry.B.Breg,” The Intel Microprocessors Architecture , Programming and Interfacing “, PHI, 2002.
8. Valvano "Embedded Microcomputer Systems" Thomson Asia PVT LTD first reprints 2001.. Readings: Web links www.ocw.nit.edu www.arm.com

EE4571	ELECTRONIC DESIGN LABORATORY – I	L	T	P	C
		0	0	2	1

OBJECTIVES:

- To design systems using PIC microcontroller
- To implement adaptive filters, periodogram and multistage multirate system in DSP processor
- To model sequential digital system using VHDL & Verilog
- To design ALU using FPGA and to design systems using 16-bit Microprocessors

Subject Code:EE4571 Subject Name: Electronic System Design Lab - I		
Course Outcome – Cos		**Cognitive Skill**
CO-01	Analyze and design systems using PIC microcontroller	An
CO-02	Analyze performance adaptive filters, periodogram and multistage multirate system in DSP processor	An
CO-03	Understand the VHDL language and apply it to the sequential circuits	A
CO-04	Understand the Verilog HDL language and apply it to the sequential circuits	U
CO-05	Design and analyse the performance of ALU using FPGA	An

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO- I	PO-J	PO-k	PO-L
CO-01	S	S	S	M	M	N	L	N	N	L	L	L
CO-02	S	S	S	M	M	N	L	N	N	L	M	L
CO-03	M	S	L	M	L	N	L	N	N	L	M	L
CO-04	M	S	L	M	L	N	L	N	N	L	L	L
CO-05	S	S	S	M	M	N	L	N	N	L	L	L

S- Strong, M- Medium, L-Low, N- Not Relevant

1. System design using PIC Microcontroller.
2. Implementation of Adaptive Filters, periodogram and multistage multirate system in DSP Processor
3. Simulation of QMF using Simulation Packages
4. Modeling of Sequential Digital system using VHDL.
5. Modeling of Sequential Digital system using Verilog.
6. Design and Implementation of ALU using FPGA.
7. Simulation of NMOS and CMOS circuits using SPICE.
8. System design using 16- bit Microprocessor.

TOTAL: 45 PERIODS

SEMESTER II

SI. NO	COURSE CODE	COURSE TITLE	L	T	P	C
THEORY						
1.	EE4504	Analysis and Design of Analog Integrated Circuits	3	0	0	3
2.	EE4505	Semiconductor Devices and Modelling	3	0	0	3
3.	EE4506	Digital Control Engineering	3	0	0	3
4.	EE4507	Advanced Embedded Systems	3	0	0	3
5.	EExxx3	Elective-III	3	0	0	3
6.	EExxx4	Elective- IV	3	0	0	3
PRACTICAL						
7.	EE4572	Electronic System Design Laboratory-II	0	0	2	1
Total			**18**	**0**	**2**	**19**

EE4504	ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS	L	T	P	C
		3	0	0	3

. **OBJECTIVES**

- To study the models for integrated circuit active devices in detail.
- To do the detailed study of current sources, biasing circuits, voltage references and output stages.
- To do the detailed study of analysis of operational amplifiers.
- To do the detailed study of analog multiplier and PLL circuits.
- To study the analog design with MOS technology in detail.

Subject Code: EE4504 Subject Name: Analysis and Design of Analog Integrated Circuits		
Course Outcome – Cos		**Cognitive Skill**
CO-01	To understand about MOS devices	R
CO-02	Analyze of difference amplifiers with active load	An
CO-03	Analyze of operational amplifiers circuit	An
CO-04	Analyze four quadrant multiplier	An
CO-05	To understand about different MOS technology	U

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO - I	PO-J	PO- k	PO –L
CO-01	S	S	S	S	M	S	N	M	N	N	S	N
CO-02	S	S	M	M	M	L	N	M	N	N	M	N
CO-03	S	S	S	M	M	M	N	M	N	N	S	N
CO-04	S	S	M	S	S	M	N	M	N	N	M	N
CO-05	S	S	M	S	L	S	N	M	N	N	M	N

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT I MODELS FOR INTEGRATED CIRCUIT ACTIVE DEVICES 9

Depletion region of a PN junction – large signal behavior of bipolar transistors- small signal model of bipolar transistor- large signal behavior of MOSFET- small signal model of the MOS transistors- short channel effects in MOS transistors – weak inversion in MOS transistors- substrate current flow in MOS transistor.

UNIT II CIRCUIT CONFIGURATION FOR LINEAR IC 9

Current sources, Analysis of difference amplifiers with active load using BJT and FET, supply and temperature independent biasing techniques, voltage references. Output stages: Emitter follower, source follower and Push pull output stages.

UNIT III OPERATIONAL AMPLIFIERS 9

Analysis of operational amplifiers circuit, slew rate model and high frequency analysis, Frequency response of integrated circuits: Single stage and multistage amplifiers, Operational amplifier noise

UNIT IV ANALOG MULTIPLIER AND PLL 9

Analysis of four quadrant and variable trans conductance multiplier, voltage controlled oscillator, closed loop analysis of PLL, Monolithic PLL design in integrated circuits: Sources of noise- Noise models of Integrated-circuit Components – Circuit Noise Calculations – Equivalent Input Noise Generators – Noise Bandwidth – Noise Figure and Noise Temperature

UNIT V ANALOG DESIGN WITH MOS TECHNOLOGY 9

MOS Current Mirrors – Simple, Cascode, Wilson and Widlar current source – CMOS Class AB output stages – Two stage MOS Operational Amplifiers, with Cascode, MOS Telescopic-Cascode Operational Amplifier – MOS Folded Cascode and MOS Active Cascode Operational Amplifiers

TOTAL: 45 PERIODS

REFERENCES

1. Gray, Meyer, Lewis, Hurst, "Analysis and design of Analog IC's", Fourth Edition, Willey International, 2002.
2. Behzad Razavi, "Principles of data conversion system design", S.Chand and company ltd, 2000
3. Nandita Dasgupata, Amitava Dasgupta,"Semiconductor Devices, Modelling and Technology", Prentice Hall of India pvt. ltd, 2004.
4. Grebene, Bipolar and MOS Analog Integrated circuit design", John Wiley & sons,Inc.,2003.
5. Phillip E.Allen Douglas R. Holberg, "CMOS Analog Circuit Design", Second Edition-Oxford University Press-2003

EE4505	SEMICONDUCTOR DEVICES AND MODELING	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To acquire the fundamental knowledge and to expose to the field of semiconductor theory and devices and their applications.
- To gain adequate understanding of semiconductor device modelling aspects, designing devices for electronic applications
- To acquire the fundamental knowledge of different semiconductor device modelling aspects.

Subject Code: EE4505	Subject Name: Semiconductor Devices and Modeling	
Course Outcome – Cos		**Cognitive Skill**
CO-01	Explore the properties of MOS capacitors.	R
CO-02	Analyze the various characteristics of MOSFET devices.	An
CO-03	Describe the various CMOS design parameters and their impact on performance of the device.	An,A
CO-04	Discuss the device level characteristics of BJT transistors.	U,R
CO-05	Identify the suitable mathematical technique for simulation	R,A

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO - I	PO- J	PO- k	PO –L
CO-01	S	S	S	S	M	S	S	M	N	N	S	N
CO-02	S	S	M	M	M	L	S	M	N	N	M	N
CO-03	S	L	S	M	M	M	L	M	N	N	S	N
CO-04	M	S	M	S	S	M	S	M	N	N	M	N
CO-05	M	S	M	S	L	S	S	M	N	N	M	N

S- Strong, M- Medium, L-Low, N- Not Relevant

UNITI MOSCAPACITORS 9

Surface Potential: Accumulation, Depletion, and Inversion, Electrostatic Potential and Charge Distribution in Silicon, Capacitances in an MOS Structure, Polysilicon-Gate Work Function and Depletion Effects, MOS under Nonequilibrium and Gated Diodes, Charge in Silicon Dioxide and at the Silicon–Oxide Interface, Effect of Interface Traps and Oxide Charge on Device Characteristics,High-FieldEffects,ImpactIonizationandAvalancheBreakdown,Band-to-BandTunneling,Tunneling into and through Silicon Dioxide, Injection of Hot Carriers from Silicon into Silicon Dioxide, High-Field Effects in Gated Diodes, Dielectric Breakdown.

UNIT II MOSFETDEVICES 9

Long-Channel MOSFETs, Drain-Current Model, MOSFETI–V Characteristics, Sub threshold Characteristics, Substrate Bias and Temperature Dependence of Threshold Voltage, MOSFET Channel Mobility, MOSFET Capacitances and Inversion-Layer Capacitance Effect, Short-Channel MOSFETs, Short-Channel Effect, Velocity Saturation and High-Field Transport Channel Length Modulation, Source–Drain Series Resistance, MOSFET Degradation and Breakdown at High Fields

UNIT III CMOS DEVICE DESIGN 9

CMOS Scaling, Constant-Field Scaling, Generalized Scaling, non scaling Effects, Threshold Voltage, Threshold-Voltage Requirement, Channel Profile Design, Nonuniform Doping, Quantum Effect on Threshold Voltage, Discrete Dopant Effects on Threshold Voltage, MOSFET Channel Length, Various Definitions of Channel Length, Extraction of the Effective Channel Length, Physical Meaning of Effective Channel Length, Extraction of Channel Length by C–V Measurements.

UNIT IV BIPOLAR DEVICES 9

n–p–n Transistors, Basic Operation of a Bipolar Transistor, Modifying the Simple Diode Theory for Describing Bipolar Transistors, Ideal Current–Voltage Characteristics, Collector Current, Base Current, Current Gains, Ideal IC–VCE Characteristics, Characteristics of a Typical n–p–n Transistor, Effect of Emitter and Base Series Resistances, Effect of Base–Collector Voltage on Collector Current, Collector Current Fall off at High Currents, Non ideal Base Current at Low Currents, Bipolar Device Models for Circuit and Time-Dependent Analyses Basic dc Model, Basic Model, Small-Signal Equivalent-Circuit Model, Emitter Diffusion Capacitance, Charge-Control Analysis, Breakdown Voltages, Common-Base Current Gain in the Presence of Base–Collector Junction Avalanche, Saturation Currents in a Transistor.

UNITV MATHEMATICALTECHNIQUES FORDEVICESIMULATIONS 9

Poisson equation, continuity equation, drift-diffusion equation, Schrodinger equation, hydro dynamic equations, trap rate, finite difference solutions totheseequationsin1D and 2Dspace,gridgeneration.

TOTAL:45PERIODS

REFERENCES:

1. YuanTaurandTakH.Ning,"FundamentalsofModernVLSIDevices",Cambridge University Press,2016.
2. A.B .Bhattacharyya “Compact MOSFET Models for VLSI Design” ,John Wiley & Sons Ltd, 2009.
3. Ansgar Jungel,“Transport Equations for Semiconductors”,Springer,2009
4. Trond Ytterdal, Yuhua Chengand Tor A. Fjeldly WayneWolf,“Device Modeling for Analog and RF CMOS Circuit Design”, John Wiley& Sons Ltd,2004
5. Selberherr,S., “Analysis and Simulation of Semiconductor Devices”,Springer-Verlag.,1984
6. Behzad Razavi ,“Fundamentals of Microelectronics”WileyStudentEdition,2nd Edition,2014
7. JPCollinge,CA Collinge, “Physics of Semiconductor devices”Springer,2002.
8. S.M.Sze,Kwok.K.NG,“ Physics of Semiconductor devices”,Springer,2006.

EE4506	DIGITAL CONTROL ENGINEERING	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To analyze the stability of discrete and digital control systems
- To design digital control system with deadbeat response and state feedback design.
- To acquire complete knowledge of design tools.

Subject Code: EE4506	**Subject Name: Digital Control Engineering**	
Course Outcome – Cos		**Cognitive Skill**
CO-01	Ability to analyze the stability of discrete and digital control systems.	An
CO-02	Ability to design digital control system with deadbeat response and state feedback design.	A
CO-03	A complete knowledge of design tools.	R,A
CO-04	State feedback design	U, An,.E
CO-05	Applied electronics design tool	R,A

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S-Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO - I	PO-J	PO- k	PO -L
CO-01	S	S	M	M	N	N	N	L	L	L	N	L
CO-02	S	S	M	M	N	N	N	L	N	L	N	L
CO-03	S	S	M	M	N	N	N	L	N	L	N	L
CO-04	S	S	M	M	N	N	N	L	L	L	N	L
CO-05	S	S	M	M	N	N	N	L	L	L	N	L

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT IINTRODUCTION TO DIGITAL CONTROL 9

Discrete time system representation, Mathematical modeling of sampling process, Data reconstruction. Modeling discrete-time systems by pulse transfer function: Review of Z-transforms, Mapping of s-plane to z-plane, Pulse transfer function, Pulse transfer function of closed loop system, Sampled signal flow graph.

UNIT II STABILITY ANALYSIS OF DISCRETE TIME SYSTEMS 9

Jury stability test, Stability analysis using bi linear transformation. Time response of discrete systems: Transient and steady state responses, Time response parameters of a prototype second order system, Design of sampled data control systems: Controller design using root locus, Nyquist stability criteria, Bode plot, Lead and Lag compensator design using Bode plot, Lag-lead compensator design in frequency domain.

UNIT IIIDEADBEAT RESPONSE DESIGN 9

Design of digital control systems with deadbeat response, Practical issues with deadbeat response design, Sampled data control systems with deadbeat response, Discrete state space model: Introduction to state variable model, Various canonical forms, Characteristic equation, state transition matrix, Solution to discrete state equation, Controllability, observability and stability of discrete state space models: Controllability, observability and stability of discrete state space models, Stability, Lyapunov stability theorem.

UNIT IV STATE FEEDBACK DESIGN 9

Pole placement by state feedback, Set point tracking controller, Full order observer, Reduced order observer, Output feedback design: Output feedback design Theory, Output feedback design Examples, Introduction to optimal control, Basics of optimal control, Performance indices, Linear Quadratic Regulator (LQR) design.

UNIT VAPPLIED ELECTRONICS DESIGN TOOL 9

Matrices and vectors, Build in function, Saving & loading data, Simulink Models: Selecting objects, Blocks, Connecting blocks, Working with signals data types, Matlab Tool Box: Control systems tool boxlinear models, MIMO models, Interconnecting linear model.

TOTAL: 45 PERIODS

REFERENCES:

1. Gopal, M., “Digital Control Engineering”, New Age International. New Delhi.
2. Kuo, B. C., “Digital Control Systems” , Oxford University Press.
3. Kuo, B. C., “Analysis and Synthesis of sampled-data control system”, PH.
4. Houpies, C. H., “Digital Control Systems (Hardware and Software)”.
5. Philips and Nagle, “Digital Control System Analysis and Design”.
6. Matlab basics, The Mathworks Inc.,2000, www.mathworks.com.

EE4507	ADVANCED EMBEDDED SYSTEMS	L	T	P	C
		3	0	0	3

OBJECTIVES

- To study the architecture and design of embedded systems with examples.
- To do the detailed study of ARM processor architecture and design with examples.
- To study the architecture of Distributed Embedded Architecture in detail with example.
- To do the detailed study of real time characteristic approaches.
- To study the Design Methodologies in detail.

Subject Code: EE4507 Subject Name: Advanced Embedded Systems

	Course Outcome – Cos	Cognitive Skill
CO-01	Know about various Requirements, Specification and Architectural Design for Embedded system design process.	U, A
CO-02	Understand and apply interfacing concepts of SHARC and ARM processors.	U, A
CO-03	Realize concepts about various Embedded Network using I2C, CAN Bus and SHARC bus for industry based applications.	R, U
CO-04	Apply the programming skills for peripheral interfacing and real time applications.	U, R,A
CO-05	Apply the concepts of RTOS for real-time systems design.	R, U

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO- C	PO-D	PO- E	PO- F	PO-G	PO-H	PO - I	PO- J	PO- k	PO -L
CO-01	S	L	S	M	L	L	S	N	L	N	L	N
CO-02	S	L	M	M	L	L	S	N	L	N	L	N
CO-03	S	L	M	M	L	L	M	N	L	N	L	N
CO-04	S	L	S	M	L	L	M	N	M	N	L	N
CO-05	S	L	S	M	L	L	M	N	M	N	L	N

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT I EMBEDDED ARCHITECTURE 9

Embedded Computers, Characteristics of Embedded Computing Applications, Challenges in Embedded Computing system design, Embedded system design process- Requirements, Specification, Architectural Design, Designing Hardware and Software Components, System Integration, Formalism for System Design- Structural Description, Behavioral Description, Design Example: Model Train Controller

UNIT II EMBEDDED PROCESSOR AND COMPUTING PLATFORM 9

ARM processor- processor and memory organization, Data operations, Flow of Control, SHARC processor- Memory organization, Data operations, Flow of Control, parallelism with instructions, CPU Bus configuration, ARM Bus, SHARC Bus, Memory devices, Input/output devices, Component interfacing, designing with microprocessor development and debugging, Design Example : Alarm Clock.

UNIT III NETWORKS 9

Distributed Embedded Architecture- Hardware and Software Architectures, Networks for embedded systems- I2C, CAN Bus, SHARC link p ports, Ethernet, Myrinet, Internet, Network-Based design- Communication Analysis, system performance Analysis, Hardware platform design, Allocation and scheduling, Design Example: Elevator Controller.

UNIT IV REAL-TIME CHARACTERISTICS 9

Clock driven Approach, weighted round robin Approach, Priority driven Approach, Dynamic Versus Static systems, effective release times and deadlines, Optimality of the Earliest deadline first (EDF) algorithm, challenges in validating timing constraints in priority driven systems, Off-line Versus On-line scheduling.

UNIT V SYSTEM DESIGN TECHNIQUES 9

Design Methodologies, Requirement Analysis, Specification, System Analysis and Architecture Design, Quality Assurance, Design Example: Telephone PBX- System Architecture, Ink jet printer- Hardware Design and Software Design, Personal Digital Assistants, Set-top Boxes.

TOTAL: 45 PERIODS

REFERENCES:

1. Wayne Wolf, Computers as Components: Principles of Embedded Computing System Design, Morgan Kaufman Publishers, 2001.
2. Jane.W.S. Liu Real-Time systems, Pearson Education Asia, 2000
3. C. M. Krishna and K. G. Shin , Real-Time Systems, ,McGraw-Hill, 1997
4. Frank Vahid and Tony Givargi Embedded System Design: A Unified Hardware/Software Introduction, s, John Wiley & Sons, 2000.

EE4572	ELECTRONIC DESIGN LABORATORY - II	L	T	P	C
		0	0	2	2

Objective:

- To design systems using PLL.
- To model the system using embedded micro controller.
- To design Non-adaptive and adaptive digital control system.

Subject Code: EE4572	**Subject Name: Electronic Design Laboratory - II**	
Course Outcome - COs		**Cognitive Skill**
CO-01	Analyze and design systems using PLL	An
CO-02	Analyze and design systems using CPLD	An
CO-03	Analyze and modelling the system using embedded micro controller	An
CO-04	Understand and design the non-adaptive digital control system	U
CO-05	Understand and design the adaptive digital control system	U

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO- I	PO- J	PO-k	PO-L
CO-01	S	S	S	S	M	N	L	L	M	S	L	N
CO-02	S	S	S	S	M	N	L	L	M	S	L	N
CO-03	S	S	L	M	L	N	L	M	L	M	M	N
CO-04	S	S	L	M	L	N	L	M	L	M	M	N
CO-05	S	S	S	S	M	N	L	L	M	S	L	N

S- Strong, M- Medium, L-Low, N- Not Relevant

List of Experiments

1. System design using PLL.
2. System design using CPLD.
3. Alarm clock using embedded micro controller.
4. Model train controller using embedded micro controller.
5. Elevator controller using embedded micro controller.
6. Simulation of Non adaptive Digital Control System using MAT LAB control system toolbox.
7. Simulation of Adaptive Digital Control System using MAT LAB control system toolbox.

TOTAL: 45 PERIODS

LIST OF PROGRAM ELECTIVES

SI. NO.	COURSE CODE	COURSE TITLE	L	T	P	C
1.	EE45A1	Robotics	3	0	0	3
2.	EE45A2	Electromagnetic Interference and Compatibility in System Design	3	0	0	3
3.	EE45A3	Low Power VLSI	3	0	0	3
4.	EE45A4	Internet Working and Multimedia	3	0	0	3
5.	EE45A5	DSP Integrated Circuits	3	0	0	3
6.	EE45A6	High Speed Switching Architecture	3	0	0	3
7.	EE45A7	CADD for VLSI Circuits	3	0	0	3
8.	EE45A8	Data Converters	3	0	0	3
9.	EE45A9	Machine Learning	3	0	0	3
10.	EE45B1	Digital Image Processing and Applications	3	0	0	3
11.	EE45B2	VLSI Design	3	0	0	3
12.	EE45B3	High Performance Communication Networks	3	0	0	3
13.	EE45B4	Embedded Analog Interfacing	3	0	0	3

EE45A1	ROBOTICS	L	T	P	C
		3	0	0	3

OBJECTIVES

Robots are slowly and steadily replacing human beings in many fields. The aim of this course is to introduce the students into this area so that they could use the same when they enter the industries. The course has been so designed to give the students an overall view of the mechanical components

1. The mathematics associated with the same.
2. Actuators and sensors necessary for the functioning of the robot.

Subject Code: EE45A1	Subject Name: ROBOTICS	
Course Outcome - COs		**Cognitive Skill**
CO-01	Gain knowledge about the characteristic features of robotics	U,R,A
CO-02	Gain knowledge in automation	U,E
CO-03	Gain knowledge of sensors and sensing devices	R,U,E
CO-04	Gain knowledge of artificial intelligence	U, An,.E
CO-05	Gain knowledge integration of robot	R,A

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO - I	PO- J	PO- k	PO -L
CO-01	S	S	M	M	L	S	S	S	S	L	S	L
CO-02	S	S	M	M	L	S	S	S	S	L	S	L
CO-03	S	L	M	M	L	S	M	S	S	L	S	L
CO-04	S	S	M	M	L	S	S	S	S	L	S	L
CO-05	S	S	M	M	L	S	S	S	S	L	S	L

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT- I: INTRODUCTION TO ROBOTICS 9

Motion - Potential Function, Road maps, Cell decomposition and Sensor and sensor planning. Kinematics. Forward and Inverse Kinematics - Transformation matrix and DH transformation. Inverse Kinematics - Geometric methods and Algebraic methods. Non-Holonomic constraints.

UNIT- II: COMPUTER VISION 9

Projection - Optics, Projection on the /Image Plane and Radiometry. Image Processing - Connectivity, Images-Gray Scale and Binary Images, Blob Filling,

Thresholding, Histogram. Convolution - Digital Convolution and Filtering and Masking Techniques. Edge Detection - Mono and Stereo Vision.

UNIT-III: SENSORS AND SENSING DEVICES 9

Introduction to various types of sensor. Resistive sensors. Range sensors - Ladar (laser distance and ranging), Sonar, Radar and Infra-red. Introduction to sensing - Light sensing, Heat sensing, Touch sensing and Position sensing.

UNIT-IV: ARTIFICIAL INTELLIGENCE 9

Uniform Search strategies - Breadth first, Depth first, Depth limited, Iterative and deepening depth first search and Bidirectional search. The A* algorithm. Planning - State-Space Planning , Plan-Space Planning, Graphplan/ SatPlan and their Comparison, Multi-agent planning 1, and Multi-agent planning 2, Probabilistic Reasoning - Bayesian Networks, Decision Trees and Bayes net inference .

UNIT-V: INTEGRATION TO ROBOT 9

Building of 4 axis or 6 axis robot - Vision System for pattern detection - Sensors for obstacle detection - AI algorithms for path finding and decision making

TOTAL: 45 PERIODS

REFERENCES:

1.Duda, Hart and Stork, *Pattern Recognition.* Wiley-Inter science, 2000.
2.Mallot, *Computational Vision: Information Processing in Perception and Visual Behavior*. Cambridge, MA: MIT Press, 2000.
3.Artificial Intelligence-A Modern Approach By Stuart Russell and Peter Norvig, Pearson Education Series in Artificial Intelligence, 2004
4. Fundamentals of Robotics, Analysis and control By Robert Schilling and Craig, Hall of India Private Limited, New Delhi, 2003.
5.Computer Vision, A modern Approach by Forsyth and Ponce, Person Education, 2003.

EE45A2	ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY IN SYSTEM DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES:

To do an advanced study of electromagnetic interference and compatibility in system design.

- To study the EMI/EMC concepts and definitions in detail.
- To do the detailed study of EMI coupling.
- To study the EMI/EMC standards and measurements in detail.
- To do the detailed study of EMI control techniques.
- To study the EMC design of PCB in detail.

Subject Code: EE45A2 Subject Name: Electromagnetic Interference And Compatibility In System Design		
Course Outcome - COs		**Cognitive Skill**
CO-01	To know about EMI Environment	U,A
CO-02	Ability to analyze Electromagnetic interference effects in PCBs	R,A
CO-03	Ability to propose solutions for minimizing EMI in PCBs	R,U,An
CO-04	EMI Specification, Standards and Limits, EMI Measurements and Control Techniques	A
CO-05	Ability to propose solutions for minimizing EMI in PCBs	U

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO - I	PO- J	PO- k	PO -L
CO-01	M	S	N	S	M	M	M	N	N	M	M	M
CO-02	M	S	N	M	M	M	M	N	N	M	M	M
CO-03	S	L	N	M	M	M	M	N	N	M	M	M
CO-04	S	M	L	N	L	M	M	N	N	M	M	M
CO-05	M	M	L	N	L	M	L	M	M	S	S	S

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT- I: EMI ENVIRONMENT 9

EMI/EMC concepts and definitions, Sources of EMI, conducted and radiated EMI, Transient EMI, Time domain Vs Frequency domain EMI, Units of measurement parameters, Emission and immunity concepts, ESD.

UNIT- II: EMI COUPLING PRINCIPLES 9

Conducted, Radiated and Transient Coupling, Common Impedance Ground Coupling, Radiated Common Mode and Ground Loop Coupling, Radiated Differential Mode Coupling, Near Field Cable to Cable Coupling, Power Mains and Power Supply coupling.

UNIT- III: EMI/EMC STANDARDS AND MEASUREMENTS9

Civilian standards - FCC, CISPR, IEC ,EN, Military standards - MIL STD 461D/462, EMI Test Instruments /Systems, EMI Shielded Chamber, Open Area Test Site, TEM Cell, Sensors/Injectors/Couplers, Test beds for ESD and EFT, Military Test Method and Procedures (462).

UNIT-IV: EMI CONTROL TECHNIQUES 9

Shielding, Filtering, Grounding, Bonding, Isolation Transformer, Transient Suppressors, Cable Routing, Signal Control, Component Selection and Mounting.

UNIT-V: EMC DESIGN OF PCBs **9**

PCB Traces Cross Talk, Impedance Control, Power Distribution Decoupling, Zoning, Motherboard Designs and Propagation Delay Performance Models.

TOTAL: 45 PERIODS

REFERENCES:

1. Henry W.Ott, "Noise Reduction Techniques in Electronic Systems", John Wiley and Sons, NewYork. 1988.
2. C.R.Paul, “Introduction to Electromagnetic Compatibility” , John Wiley and Sons, Inc, 1992
3. V.P.Kodali, "Engineering EMC Principles, Measurements and Technologies", IEEE Press, 1996.
4. Bernhard Keiser, "Principles of Electromagnetic Compatibility", Artech house, 3rd Ed, 1986.
5.
6.

EE45A3	LOW POWER VLSI	L	T	P	C
		3	0	0	3

OBJECTIVES:

- Identify sources of power in an IC.
- Identify the power reduction techniques based on technology independent and technology dependent
- Power dissipation mechanism in various MOS logic style.
- Identify suitable techniques to reduce the power dissipation.
- Design memory circuits with low power dissipation.

Subject Code: EE45A3	Subject Name: LOW POWER VLSI	
	Course Outcome – Cos	**Cognitive Skill**
CO-01	To understand the basics of low power design	U
CO-02	Analysis of Basic low power process and devices	An
CO-03	Evaluation of device modeling and behavior	E
CO-04	To remember the Logic gates	R
CO-05	To understand the Principle Flip Flops	U

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO- C	PO-D	PO- E	PO- F	PO-G	PO-H	PO - I	PO- J	PO- k	PO -L
CO-01	M	L	N	N	N	S	S	N	N	N	S	N
CO-02	S	N	N	N	N	L	S	N	N	N	M	N
CO-03	L	S	N	N	N	M	L	N	N	N	S	N
CO-04	S	L	N	S	N	M	S	N	N	N	M	N
CO-05	S	N	N	S	N	S	S	N	N	N	M	N

S- Strong, M- Medium, L-Low, N- Not Relevant

UNITI POWER DISSIPATION IN CMOS 9

Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOSFET devices – Basic principle of low power design.

UNITII POWER OPTIMIZATION 9

Logic level power optimization – Circuit level low power design – circuit techniques for reducing power consumption in adders and multipliers.

UNITIII DESIGN OF LOW POWER CMOS CIRCUITS 9

Computer arithmetic techniques for low power system – reducing power consumption in memories –low power clock, Inter connect and layout design – Advanced techniques –Special techniques.

UNITIV POWER ESTIMATION 9

Power Estimation techniques – logic power estimation – Simulation power analysis –Probabilistic power analysis.

UNITV SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER 9

Synthesis for low power – Behavioral level transform – software design for low power.

TOTAL: 45 PERIODS

TEXT BOOKS:

1. CMOS/BiCMOS ULSI low voltage, low power by Yeo Rofail/ Gohl(3 Authors) - Pearson Education Asia 1st Indian reprint, 2002

REFERENCES:

1. Kaushik Roy and S.C.Prasad, “Low power CMOS VLSI circuit design”, Wiley, 2000.

2. Dimitrios Soudris, Chirstian Pignet, Costas Goutis, "Designing CMOS Circuits for Low Power",Kluwer, 2002.
3. J.B.Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley 1999.
4. A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design", Kluwer,1995.
5. Gary Yeap, "Practical low power digital VLSI design", Kluwer, 1998.
6. Abdelatif Belaouar, Mohamed.I.Elmasry, "Low power digital VLSI design", Kluwer, 1995.
7. James B.Kulo, Shih-Chia Lin, "Low voltage SOI CMOS VLSI device devices and Circuits", John Wiley and sons, inc. 2001.

EE45A4	ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY IN SYSTEM DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES

- To introduce the characteristics of text, graphics, video and speech.
- To teach techniques for efficient transmission of multimedia signals over networks.
- To introduce different network standards and parameters for quality of service.

Subject Code: EE45A4 Subject Name: INTERNET WORKING AND MULTIMEDIA
Subject Name:
Subject Name:

Course Outcome – Cos		Cognitive Skill
CO-01	Understanding about the architecture and models of multimedia communication.	U, R
CO-02	Understand and design end to end of broadband network services.	R,A
CO-03	Build the multicast routing and guaranteed service models.	A
CO-04	Provide the end to end solutions for multimedia services on demand.	An
CO-05	To built the various Multimedia Communication tasks.	A

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO - I	PO- J	PO- k	PO -L
CO-01	S	M	S	L	S	M	L	M	N	L	L	N
CO-02	L	S	M	L	M	S	M	M	N	N	L	N
CO-03	M	L	L	N	S	M	S	S	N	L	M	N
CO-04	L	S	S	N	L	L	S	S	N	M	S	N
CO-05	S	M	N	N	M	M	M	M	N	M	M	N

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT- I: MULTIMEDIA NETWORKING 9

Digital sound, video and graphics, basic multimedia networking, multimedia characteristics, evolution of Internet services model, network requirements for audio/video transform, multimedia coding and compression for text, image, audio and video.

UNIT- II : BROAD BAND NETWORK TECHNOLOGY 9

Broadband services, ATM and IP , IPV6, High speed switching, resource reservation, Buffer management, traffic shaping, caching, scheduling and policing, throughput, delay and jitter performance.

UNIT-III: MULTICAST AND TRANSPORT PROTOCOL 9

Multicast over shared media network, multicast routing and addressing, scaping multicast and NBMA networks, Reliable transport protocols, TCP adaptation algorithm, RTP, RTCP.

UNIT- IV: MEDIA - ON – DEMAND 9

Storage and media servers, voice and video over IP, MPEG over ATM/IP, indexing synchronization of requests, recording and remote control.

UNIT –V: APPLICATIONS 9

MIME, Peer-to-peer computing, shared application, video conferencing, centralized and distributed conference control, distributed virtual reality, light weight session philosophy.

TOTAL: 45 PERIODS

REFERENCES:

1. Jon Crowcroft, Mark Handley, Ian Wakeman. Internetworking Multimedia, Harcourt Asia Pvt.Ltd.Singapore, 1998.
2. B.O. Szuprowicz, Multimedia Networking, McGraw Hill, NewYork. 1995.
3. Tay Vaughan, Multimedia making it to work, 4ed,Tata McGrawHill, NewDelhi, 2000.

EE45A5	DSP INTEGRATED CIRCUITS	L	T	P	C
		3	0	0	3

OBJECTIVES

- To familiarize the concept of DSP and DSP algorithms.
- Introduction to Multirate systems and finite word length effects.
- To know about the basic DSP processor architectures and the synthesis of the processing elements.
- To gather an idea about the VLSI circuit layout design styles.

Subject Code: EE45A5	Subject Name : DSP INTEGRATED CIRCUITS	
Course Outcome – Cos		**Cognitive Skill**
CO-01	Gain knowledge in DSP and DSP algorithms	U,R,A
CO-02	Gain knowledge in digital filters and finite word length effects	U,E
CO-03	Gain knowledge in DSP architecture	R,U
CO-04	Gain knowledge in synthesis of DSP architecture	U, S.E
CO-05	Gain knowledge integrated circuit design	R,A

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO - I	PO- J	PO- k	PO -L
CO-01	S	S	M	M	N	N	L	L	L	L	S	L
CO-02	S	S	M	M	N	N	L	M	N	L	S	L
CO-03	S	S	M	M	N	N	S	L	N	L	S	L
CO-04	S	S	M	M	N	N	S	L	L	L	S	L
CO-05	S	S	M	M	N	N	M	L	L	L	S	L

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT- I : INTRODUCTION TO DSP INTEGRATED CIRCUITS 9

Introduction to Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal-processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT-The Fast Fourier Transform Algorithm, Image coding, Discrete cosine transforms, Standard digital signal processors, Application specific IC's for DSP, DSP systems, DSP system design, Integrated circuit design.

UNIT- II: DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS 9

FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multirate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multirate filters. Finite word length effects –Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

UNIT-III: DSP ARCHITECTURES 9

DSP system architectures, Standard DSP architecture-Harvard and Modified Harvard architecture.TMS320C54x and TMS320C6x architecture, Motorola DSP56002 architecture, Ideal DSP architectures, Multiprocessors and multicomputers, Systolic and Wave front arrays, Shared memory architectures.

UNIT- IV: SYNTHESIS OF DSP ARCHITECTURES AND ARITHMETIC UNIT 9

Synthesis: Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs. Arithmetic Unit : Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit-Serial arithmetic, Digit Serial arithmetic, CORDIC Algorithm, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator.

UNIT V CASE STUDY-INTEGRATED CIRCUIT DESIGN 9

Layout of VLSI circuits, Layout Styles, Case Study: FFT processor, DCT processor and Interpolator.

TOTAL: 45 PERIODS

REFERENCES:

1. Lars Wanhammer, "DSP Integrated Circuits", Academic press, New York, 1999.
2. John J. Proakis, Dimitris G. Manolakis, "Digital Signal Processing", Pearson Education,2002.
3. B.Venkatramani, M.Bhaskar, "Digital Signal Processors", Tata McGraw-Hill, 2002.
4. Emmanuel C. Ifeachor, Barrie W. Jervis, " Digital signal processing – A practical approach", Tata McGraw-Hill, 2002.
5. Keshab K.Parhi, "VLSI Digital Signal Processing Systems design and Implementation", John Wiley & Sons, 1999.

EE45A6	HIGH SPEED SWITCHING ARCHITECTURE	L	T	P	C
		3	0	0	3

OBJECTIVES

To highlight the features of different technologies involved in High Speed Networking and their performance.

- Students will get an introduction about various high speed networks.
- Students will be provided with an up-to-date survey of developments in High Speed Networks.
- Enable the students to know techniques involved in LAN switching and ATM switching.
- Students will get an introduction about various Queuing techniques involved in high speed networks

Subject Code: EE45A6	Subject Name : High Speed Switching Architecture	
Course Outcome - COs		**Cognitive Skill**
CO-01	To understand the basic concepts of High-Speed Networks.	U
CO-02	Apply the various switching techniques in ATM and LAN networks	A
CO-03	Analyze various queuing techniques in ATM switches.	An
CO-04	Design and develop the IP switching networks	An
CO-05	Understand various switching networks	U

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO- I	PO- J	PO-k	PO-L
CO-01	L	L	S	L	S	L	M	N	S	N	S	M
CO-02	S	L	M	S	S	M	S	N	M	N	M	L
CO-03	M	M	M	S	L	M	L	N	S	N	M	L
CO-04	M	M	M	S	L	M	L	N	S	N	M	L
CO-05	L	L	S	L	S	L	M	N	S	N	S	M

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT- I: HIGH SPEED NETWORK 9

Introduction- LAN, WAN, Network evolution through ISDN to B-ISDN, Transfer mode and control of B-ISDN, SDH multiplexing structure, ATM standard, ATM adaptation layers.

UNIT- II: LAN SWITCHING TECHNOLOGY 9

Switching Concepts, switch forwarding techniques, switch path control, LAN Switching, cut through forwarding, store and forward, virtual LANs

UNIT- III: ATM SWITCHING ARCHITECTURE 9

Switch model, Blocking networks - basic - and- enhanced banyan networks, sorting networks - merge sorting, rearrangeable networks - full-and- partial connection networks, non blocking networks - Recursive

network construction, comparison of non-blocking network, Switching with deflection routing - shuffle switch, tandem banyan

UNIT- IV: QUEUES IN ATM SWITCHES 9

Internal Queueing -Input, output and shared queueing, multiple queueing networks – combined Input, output and shared queueing - performance analysis of Queued switches.

UNIT-V: IP SWITCHING 9

Addressing model, IP Switching types - flow driven and topology driven solutions, IP Over ATM address and next hop resolution, multicasting, Ipv6 over ATM.

TOTAL: 45 PERIODS

REFERENCES:

1. Achille Pattavina, Switching Theory: Architectures and performance in Broadband ATM networks "John Wiley & Sons Ltd, New York. 1998
2. Christopher Y Metz, Switching protocols & Architectures, McGraw - Hill Professional Publishing, NewYork.1998.
3. Rainer Handel, Manfred N Huber, Stefan Schroder, ATM Networks - Concepts Protocols, Applications III Edition, Addison Wesley, New York. 1999.
4. John A.Chiong: Internetworking ATM for the internet and enterprise networks. McGraw Hill, New York, 1998.

EE45A7	CADD FOR VLSI CIRCUITS	L	T	P	C
		3	0	0	3

OBJECTIVES

- The design of all VLSI circuits is carried out by making extensive use Computer Aided Design (CAD) VLSI design tool. Due to continuous scaling of semiconductor technology, most of the VLSI designs employ millions of transistors and circuits of this size can only be carried out with the aid of CAD VLSI design tools.
- The VLSI design professional needs to have a good understanding of the operation of these CAD VLSI design tools as these are developed primarily for and by the VLSI design professionals.

Subject Code : EE45A7	Subject Name :CADD for VLSI Circuits	
Course Outcome – Cos		**Cognitive Skill**
CO-01	Design advanced electronics systems	U
CO-02	Evaluate and analyze the systems in VLSI design environments	E

CO-03	Apply advanced technical knowledge in multiple contexts	A
CO-04	systematic study on significant research topic within the field of VLSI	An
CO-05	Conduct an organized and systematic study on significant research topic within the allied field.	An

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO- I	PO- J	PO-k	PO-L
CO-01	L	L	S	L	S	L	M	S	N	N	S	M
CO-02	S	M	M	M	L	S	L	M	N	L	M	M
CO-03	S	L	M	S	S	M	S	N	M	N	M	L
CO-04	M	M	M	S	L	M	L	N	S	N	M	L
CO-05	L	L	S	L	S	L	M	N	S	N	S	M

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT- I: VLSI DESIGN METHODOLOGIES 9

Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity – Tractable and Intractable problems - general purpose methods for combinatorial optimization.

UNIT- II: DESIGN RULES 9

Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation - Placement algorithms – partitioning.

UNIT- III: FLOOR PLANNING 9

Floor planning concepts - shape functions and floorplan sizing - Types of local routing problems -Area routing - channel routing - global routing - algorithms for global routing.

UNIT- IV: SIMULATION 9

Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

UNIT- V: MODELLING AND SYNTHESIS 9

High level Synthesis - Hardware models - Internal representation - Allocation assignment and scheduling - Simple scheduling algorithm - Assignment problem - High level transformations.

TOTAL: 45 PERIODS

REFERENCES:

1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2002.
2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.

EE45A8	DATA CONVERTERS	L	T	P	C
		3	0	0	3

OBJECTIVES

- Analog to Digital (AD) and Digital to Analog (DA) converters constitute a very important building block in all electronics systems. It is these blocks which provide the crucial interface between the primarily analog real world signals and the predominantly digital electronic systems.
- These are critical blocks which are utilized in all major industrial sectors including computers, wireless communication, audio and video systems, biomedical systems, aerospace and automotive systems and so on. There are a few established circuit architectures and principles for design of AD and DA converters.

Subject Code: EE45A8	**Subject Name : Data Converters**	
Course Outcome – Cos		**Cognitive Skill**
CO-01	Evolution of converters	R
CO-02	Compute Switched-capacitor amplifiers	A
CO-03	performance metrics of ADCs and DACs	A
CO-04	Pipelined Architecture	A
CO-05	Sigma delta modulator characteristics.	S

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO- C	PO-D	PO- E	PO- F	PO-G	PO-H	PO - I	PO- J	PO- k	PO -L
CO-01	S	S	S	S	S	S	S	L	L	L	L	L
CO-02	S	M	M	S	M	M	M	M	N	N	N	N
CO-03	S	S	S	M	M	M	M	L	N	N	N	N
CO-04	S	M	M	M	M	S	S	L	N	N	N	N
CO-05	S	S	S	S	S	M	M	L	N	N	N	N

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT- I : INTRODUCTION AND CHARACTERISTICS OF AD/DA CONVERTER CHARACTERISTICS 9

Evolution, types and applications of AD/DA characteristics, issues in sampling, quantization and reconstruction, oversampling and antialiasing filters.

UNIT- II: SWITCH CAPACITOR CIRCUITS AND COMPARATORS 9

Switched-capacitor amplifiers, switched capacitor integrator, switched capacitor common mode feedback. Single stage amplifier as comparator, cascaded amplifier stages as comparator, latched comparators. offset cancellation, Op Amp offset cancellation, Calibration techniques.

UNIT- III: NYQUIST RATE D/A CONVERTERS 9

Current Steering DACs, capacitive DACs, Binary weighted versus thermometer DACs, issues in current element matching, clock feed through, zero order hold circuits, DNL, INL and other performance metrics of ADCs and DACs.

UNIT- IV: PIPELINE AND OTHER ADCs 9

Performance metrics, Flash architecture, Pipelined Architecture, Successive approximation architecture, Time interleaved architecture.

UNIT –V: SIGMA DELTA CONVERTERS 9

STF, NTF, first order and second order sigma delta modulator characteristics, Estimating the maximum stable amplitude, CTDSMs, Op amp nonlinearities.

TOTAL: 45 PERIODS

REFERENCES:

1. Behzad Razavi, “Principles of data conversion system design”, IEEE press, 1995.
2. M. Pelgrom, Analog-to-Digital Conversion, Springer, 2010.
3. Rudy van de Plassche, “CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters” Kluwer Acedamic Publishers, Boston, 2003.

4. R. Schreier, G. Temes, Understanding Delta-Sigma DataConverters, Wiley-IEEE Press, 2004
5. J. G. Proakis, D. G. Manolakis, Digital Signal Processing,Prentice Hall, 1995
6. VLSI Data Conversion Circuits EE658 recorded lectures available at http://www.ee.iitm.ac.in/~nagendra/videolecture

EE45A9	MACHINE LEARNING	L	T	P	C
		3	0	0	3

OBJECTIVES

- To understand the need for machine learning for various problem solving
- To study the various supervised, semi-supervised and unsupervised learning algorithms in machine learning
- To understand the latest trends in machine learning
- To design appropriate machine learning algorithms for problem solving

Subject Code: EE45A9	**Subject Name: Machine Learning**	
Course Outcome – Cos		**Cognitive Skill**
CO-01	Learning problems, perspectives and Issues	R, U
CO-02	Ability to understand neural networks and genetic algorithm models of evaluation.	A
CO-03	Understand Bayesian learning	U, An
CO-04	Evaluate and define instant based learning	E
CO-05	Study the rules and regulations of advanced learning	A

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO- C	PO-D	PO- E	PO- F	PO-G	PO-H	PO - I	PO- J	PO- k	PO -L
CO-01	S	S	S	S	S	S	S	L	L	L	L	L

CO-02	S	M	M	S	M	M	M	M	N	N	N	N
CO-03	S	S	S	M	M	M	M	L	N	L	N	N
CO-04	S	M	M	M	M	S	S	L	N	L	N	N
CO-05	S	S	S	S	S	M	M	L	N	L	N	N

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT I INTRODUCTION **9**

Learning Problems – Perspectives and Issues – Concept Learning – Version Spaces and Candidate Eliminations – Inductive bias – Decision Tree learning – Representation – Algorithm – Heuristic Space Search.

UNIT II NEURAL NETWORKS AND GENETIC ALGORITHMS **9**

Neural Network Representation – Problems – Perceptron – Multilayer Networks and Back Propagation Algorithms – Advanced Topics – Genetic Algorithms – Hypothesis Space Search – Genetic Programming – Models of Evaluation and Learning.

UNIT III BAYESIAN AND COMPUTATIONAL LEARNING **9**

Bayes Theorem – Concept Learning – Maximum Likelihood – Minimum Description Length Principle – Bayes Optimal Classifier – Gibbs Algorithm – Naïve Bayes Classifier – Bayesian Belief Network – EM Algorithm – Probability Learning – Sample Complexity – Finite and Infinite Hypothesis Spaces – Mistake Bound Model.

UNIT IV INSTANT BASED LEARNING **9**

K- Nearest Neighbour Learning – Locally weighted Regression – Radial Basis Functions – Case Based Learning.

UNIT V ADVANCED LEARNING **9**

Learning Sets of Rules – Sequential Covering Algorithm – Learning Rule Set – First Order Rules – Sets of First Order Rules – Induction on Inverted Deduction – Inverting Resolution – Analytical Learning – Perfect Domain Theories – Explanation Base Learning – FOCL Algorithm – Reinforcement Learning – Task – Q-Learning – Temporal Difference Learning.

TOTAL :45 PERIODS

REFERENCES

1. Tom M. Mitchell, ―Machine Learning, McGraw-Hill Education (India) Private Limited, 2013.
2. Ethem Alpaydin, ―Introduction to Machine Learning (Adaptive Computation and Machine Learning), The MIT Press 2004.
3. Stephen Marsland, ―Machine Learning: An Algorithmic Perspective‖, CRC Press, 2009.

EE45B1	DIGITAL IMAGE PROCESSING AND APPLICATIONS	L	T	P	C
		3	0	0	3

OBJECTIVES:

To introduce the student to various image processing techniques such as enhancements, segmentation, compression etc.

- To study the image fundamentals and mathematical transforms necessary for image processing.
- To study the image enhancement techniques
- To study image restoration procedures.
- To study the image compression procedures.
- To study the image segmentation and representation techniques.

Subject Code: EE45B1	Subject Name: Digital Image Processing and Applications	
Course Outcome – Cos		**Cognitive Skill**
CO-01	Review the fundamental concepts of a digital image processing system.	R
CO-02	Analyze images in the frequency domain using various transforms	An
CO-03	Evaluate the techniques for image enhancement and image restoration	E
CO-04	Categorize various compression techniques	U
CO-05	Interpret image segmentation and representation techniques.	R

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO- C	PO-D	PO- E	PO- F	PO-G	PO-H	PO - I	PO- J	PO- k	PO -L
CO-01	S	N	N	L	M	M	L	S	L	M	S	M
CO-02	M	M	S	L	M	M	S	S	L	M	S	M
CO-03	M	S	M	L	M	M	M	M	M	M	M	M
CO-04	M	S	N	L	M	M	L	M	M	S	M	M
CO-05	N	M	N	L	M	M	M	M	L	L	S	M

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT- I: DIGITAL IMAGE FUNDAMENTALS AND TRANSFORMS 9

Elements of digital image processing systems, Elements of visual perception, psycho visual model, brightness, contrast, hue, saturation, mach band effect, Image Transforms - Discrete Cosine Transform, Walsh Transform, Hadamard Transform, Slant Transform, Haar Transform Discrete Wavelet Transform.

UNIT –II: IMAGE ENHANCEMENT AND RESTORATION 9

Histogram modification and specification techniques, Noise distributions, Spatial averaging, Homomorphic filtering, Pseudo Color image processing, Full color image processing. Image Restoration – degradation model, Unconstrained and Constrained restoration, Wiener filtering, Geometric transformations – spatial transformations, Gray-Level interpolation.

UNIT- III: IMAGE SEGMENTATION, REPRESENTATION AND DESCRIPTION 9

Point, Line and Edge detection – Edge linking via Hough transform – Thresholding – Region based segmentation, Region growing, Region splitting and Merging – Image representation schemes – Boundary descriptors – Regional descriptors – Relational descriptors.

UNIT –IV: IMAGE COMPRESSION 9

Need for data compression, Huffman, Shannon Fano Coding, Run Length Encoding, Shift codes, Arithmetic coding, Vector Quantization, Block Truncation Coding. Transform Coding – DCT, JPEG, MPEG Standards.

UNIT –V: APPLICATIONS 9

Imaging Applications: Patterns and Pattern classes, Optical character Recognition- Rule based Character Recognition- Face and Facial feature Extraction - Video motion Analysis- Image Fusion- Watermarking – spatial & frequency domain

TOTAL: 45 PERIODS

REFERENCES:

1. Rafael C. Gonzalez, Richard E.Woods, 'Digital Image Processing', Pearson Education, Inc., Second Edition, 2004.
2. Anil K. Jain, 'Fundamentals of Digital Image Processing', Prentice Hall of India, 2002.
3. David Salomon : Data Compression – The Complete Reference, Springer Verlag New York Inc., 2nd Edition, 2001
4. Rafael C. Gonzalez, Richard E.Woods, Steven Eddins, ' Digital Image Processing using MATLAB', Pearson Education, Inc., 2004.
5. William K.Pratt, ' Digital Image Processing', John Wiley, NewYork, 2002.
6. MilmanSonka, Vaclav Hlavac, Roger Boyle, 'Image Processing, Analysis, and Machine Vision', Brooks/Cole, Vikas Publishing House, II ed., 1999.
7. Sid Ahmed, M.A., 'Image Processing Theory, Algorithms and Architectures', McGrawHill, 1995.
8.

EE45B2	VLSI DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES

- Analyze the characteristics of MOS transistor.
- Understand various CMOS fabrication techniques.
- Identify latch up problems in CMOS circuits.
- Illustrate the concepts of CMOS inverters and their sizing methods.
- Estimate Power and delay in CMOS circuits.

Subject Code: EE45B2	**Subject Name: VLSI DESIGN**	
Course Outcome – Cos		**Cognitive Skill**
CO-01	Understand the Conventional design procedure MOS transistor theory and process technology	U, A
CO-02	Understand the basics of inverters and logic gates.	U, A
CO-03	Design the circuit and estimate the performance of the circuit	R, U
CO-04	Understand and remember system components using VLSI techniques.	U, R,A
CO-05	Design the digital components using verilog hardware description language	R, U

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO- C	PO-D	PO- E	PO- F	PO-G	PO-H	PO - I	PO- J	PO- k	PO -L
CO-01	S	S	L	M	L	L	S	N	L	N	L	L
CO-02	S	M	L	M	L	L	S	N	L	N	L	L
CO-03	S	M	L	M	S	L	S	N	M	N	L	L
CO-04	M	S	L	M	S	L	S	N	M	N	L	L
CO-05	M	S	L	M	S	L	S	N	M	N	l	L

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT I MOS TRANSISTOR THEORY 9

NMOS and PMOS transistors, CMOS logic, MOS transistor theory – Introduction, Enhancement mode transistor action, Ideal I-V characteristics, DC transfer characteristics, Threshold voltage- Body effect- Design equations- Second order effects. MOS models and small signal AC characteristics, Simple MOS capacitance Models, Detailed MOS gate capacitance model, Detailed MOS Diffusion capacitance model..

UNIT II CMOS TECHNOLOGY AND DESIGN RULE 9

CMOS fabrication and Layout, CMOS technologies, P -Well process, N -Well process, twin -tub process, MOS layers stick diagrams and Layout diagram, Layout design rules, Latch up in CMOS circuits, CMOS process enhancements, Technology – related CAD issues, Fabrication and packaging.

UNIT III INVERTERS AND LOGIC GATES 9

NMOS and CMOS Inverters, Inverter ratio, DC and transient characteristics , switching times, Super buffers, Driving large capacitance loads, CMOS logic structures , Transmission gates, Static CMOS design, dynamic CMOS design..

UNIT IV CIRCUIT CHARACTERISATION AND PERFORMANCE ESTIMATION. 9

Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistor sizing, power dissipation and design margining. Charge sharing .Scaling.

UNIT V VLSI SYSTEM COMPONENTS CIRCUITS AND SYSTEM LEVEL PHYSICAL DESIGN 9

Multiplexers, Decoders , comparators, priority encoders , shift registers, Arithmetic circuits-Ripple carry adders, Carry look ahead adders, High-speed adders, Multipliers. Physical design – Delay modelling, cross talk, floor planning, power distribution. Clock distribution. Basics of CMOS testing.

TOTAL: 45 PERIODS

REFERENCES:

1. Neil H.E. Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, Pearson Education ASIA, 2nd edition, 2000.
2. John P.Uyemura "Introduction to VLSI Circuits and Systems", John Wiley & Sons, Inc., 2002.
3. Eugene D. Fabricius, Introduction to VLSI Design McGraw Hill International Editions, 1990.
4. Pucknell, "Basic VLSI Design", Prentice Hall of India Publication, 1995.
5. Wayne Wolf "Modern VLSI Design System on chip. Pearson Education.2002.

EE45B3	HIGH PERFORMANCE COMMUNICATION NETWORKS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To ensure a comprehensive understanding of high speed computer network architectures

- To study mathematical models related to network performance analysis.
- To focus on current and emerging networking technologies.

Subject Code: EE 45B3 Subject Name: High Performance Communication Networks		
Course Outcome – Cos		**Cognitive Skill**
CO-01	To design High performance computer networks.	U, A
CO-02	To design and implement CAC protocols in multimedia networks.	U, A
CO-03	Design and implement network protocols in HPCN.	R, U
CO-04	Analyse performance of network related issues using mathematical models.	An,A
CO-05	Compare the various methods of providing connection-oriented services over an advanced network with reference to MPLS, VPN.	R, U

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO- C	PO-D	PO- E	PO- F	PO-G	PO-H	PO - I	PO- J	PO- k	PO -L
CO-01	S	S	L	M	L	L	S	N	M	N	L	L
CO-02	S	S	L	M	L	L	S	N	M	N	L	L
CO-03	S	M	L	M	L	L	S	N	M	N	L	L
CO-04	S	M	L	M	L	L	S	N	M	N	L	L
CO-05	S	M	L	M	L	L	S	N	M	N	l	L

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT I PACKET SWITCHED NETWORKS 9

OSI and IP models, Ethernet (IEEE 802.3), Token ring (IEEE 802.5), Wireless LAN (IEEE 802.11) DQDB, ISDN and Broadband ISDN architecture and Protocols.

UNIT II ATM AND FRAME RELAY 9

ATM: Main features-addressing, signaling and routing, ATM header structure-adaptation layer, management and control, ATM switching and transmission.

Frame Relay: Protocols and services, Congestion control, Internetworking with ATM, Internet and ATM, Frame relay via ATM.

UNIT III ADVANCED NETWORK ARCHITECTURE 9

IP forwarding architectures overlay model, Multi Protocol Label Switching (MPLS), integrated services in the Internet, VPN-Remote-Access VPN, site-to-site VPN, Tunneling to PPP, Security in VPN.

UNIT IV BLUE TOOTH TECHNOLOGY 9

The Blue tooth module-Protocol stack Part I: Antennas, Radio interface, Base band, The Link controller, Audio, The Link Manager, The Host controller interface; The Blue tooth module-Protocol stack Part I: Logical link control and adaptation protocol.

UNIT V MULTIMEDIA NETWORKING APPLICATIONS 9

Streaming stored Audio and Video, Best effort service, protocols for real time interactive applications, Beyond best effort, scheduling and policing mechanism, integrated services, Resource Reservation Protocol (RSVP), Differentiated services

TOTAL: 45 PERIODS

REFERENCES:

1. Aunurag Kumar, D. Manjunath, Joy Kuri, "Communication Networking", Morgan Kaufmann Publishers, 2011.
2. J.F. Kurose & K.W. Ross, "Computer Networking- A Top Down Approach Featuring the Internet", Pearson, 2nd Edition, 2003.
3. Nader F.Mir, "Computer and Communication Networks", Pearson Education, 2009.
4. Walrand .J. Varatya, "High Performance Communication Network", Morgan Kaufmann – Harcourt Asia Pvt. Ltd., 2nd Edition, 2000.
5. HersentGurle& petit, "IP Telephony, Packet Pored Multimedia Communication Systems", Pearson Education 2003.
6. Fred Halsall and Lingana Gouda Kulkarni, "Computer Networking and the Internet", Fifth Edition, Pearson Education, 2012.
7. Larry L.Peterson& Bruce S.David, "Computer Networks: A System Approach"- Morgan Kaufmann Publisher, 1996.

EE45B4	EMBEDDED ANALOG INTERFACING	L	T	P	C
		3	0	0	3

OBJECTIVES

To do an advanced study of measurement system design, analog to digital converters, sensors and peripherals, output control methods and micro controller interfacing

- To do a detailed study of measurement system design.
- To study the analog to digital converters in detail.

- To study the sensors and peripherals in detail.
- To do the detailed study of output control methods.
- To study in detail about the micro controller interfacing.

Subject Code: EE45B4	**Subject Name : Embedded Analog Interfacing**	
	Course Outcome – Cos	**Cognitive Skill**
CO-01	Understand the characteristics of measurement	U, A
CO-02	Understand the concept of analog to digital converters.	U, A
CO-03	Understand the concept of sensors and peripherals	R, U
CO-04	Understand and various control methods.	U, R,A
CO-05	Understand microcontroller interfacing.	R, U

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO- C	PO-D	PO- E	PO- F	PO-G	PO-H	PO - I	PO- J	PO- k	PO -L
CO-01	S	L	M	M	S	L	S	N	M	N	L	N
CO-02	S	L	M	M	L	L	S	N	M	N	L	N
CO-03	S	S	M	S	L	L	N	N	M	N	L	N
CO-04	S	S	M	S	S	L	N	N	M	N	L	N
CO-05	S	L	M	S	S	L	S	N	M	N	l	N

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT –I:MEASUREMENT SYSTEM DESIGN **9**

Characteristics of Instrumentation – Measurement accuracy – Measurement standards - Dynamic Range – Calibration – Bandwidth – Digital interfacing advantages

UNIT- II:ANALOG-TO-DIGITAL CONVERTERS

Types of ADCs - ADC Comparison - Sample and Hold - ADC Types - Flash ADC - Successive Approximation ADC - Dual-Slope (Integrating) ADC - Sigma-Delta ADC - Microprocessor Interfacing - Clocked Interfaces - Serial Interfaces – Integrated ADC Embedded Controllers

UNIT- III:SENSORS & PERIPHERALS 9

Temperature Sensors - Optical Sensors – CCDs - Magnetic Sensors - Motion/Acceleration Sensors - Strain Gauges - Solenoids – Heaters – Coolers – LEDs – DACs - Digital Potentiometers - Analog Switches - Stepper Motors - DC Motors

UNIT- IV:OUTPUT CONTROL METHODS 9

Measuring Period versus Frequency - Voltage-to-Frequency Converters - Open-Loop Control - Negative Feedback and Control - Microprocessor-Based Systems- On-Off Control - Proportional Control - Proportional, Integral, Derivative Control - Motor Control - Predictive Control - Measuring and Analyzing Control Loops

UNIT- V :MICROCONTROLLER INTERFACING 9

Standard Interfaces - IEEE 1451.2 - 4–20 ma Current Loop – Fieldbus - Microcontroller Supply and Reference - Resistor Networks - Multiple Input Control -AC Control - Voltage Monitors and Supervisory Circuits - Driving Bipolar Transistors/ MOSFET- Reading Negative Voltages – PWM based control

TOTAL: 45 PERIODS

REFERENCES:

1. Analog Interfacing to Embedded Microprocessor Systems by Stuart R. Ball.
2. The measurement, Instrumentation, & sensors Handbook by John G. Webster.
3. Microcontroller-Based Temperature Monitoring and Control by by Dogan Ibrahim.